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EXAMINER	
BARNES, CRYSTAL J	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,275	LAW ET AL.	
	Examiner	Art Unit	
	Crystal J. Barnes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-35* is/are rejected.

7)☒ Claim(s) *4,11 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/12/03 & 5/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is an initial Office Action upon examination of the above-identified application on the merits. Claims 1-35 are pending in this application.

Information Disclosure Statement

2. The examiner has considered the information disclosure statements (IDS) submitted on 12 December 2003 and 6 May 2005.

Claim Objections

3. Applicant is advised that should claim 11 be found allowable, claim 13 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 14-19 and 21-33 are rejected under 35 U.S.C. 102(e) as being anticipated by USPN 6,792,550 B2 to Osecky et al.

As per claim 1, the Osecky et al. reference discloses a method for servicing a cooling system for an electronic device, the method comprising: switching the electronic device (see column 3 line 50, "CPUs 12 and 14") from a normal operating mode (see column 8 lines 26-28, "normal mode") wherein the electronic device ("CPUs 12 and 14") generates heat to a reduced heat generating mode (see column 3 lines 55-58, "low power mode") wherein the electronic device ("CPUs 12 and 14") generates heat at a reduced rate; continuing to operate the electronic device ("CPUs 12 and 14") in the reduced heat generating mode ("low power mode") while

the cooling system (see column 4 lines 6-10, "cooling devices 28, 30 ") is being serviced (see column 7 lines 47-62, "operator notification"); and subsequently switching the electronic device ("CPUs 12 and 14") from the reduced heat generating mode ("low power mode") to the normal operating mode ("normal mode").

As per claim 2, the Osecky et al. reference discloses switching the electronic device ("CPUs 12 and 14") from the normal operating mode ("normal mode") to the reduced heat generating mode ("low power mode") comprises reducing a clock frequency (see column 7 lines 19-21, "reducing the clock speed") applied to the electronic device ("CPUs 12 and 14").

As per claim 14, the Osecky et al. reference discloses switching the electronic device ("CPUs 12 and 14") from the normal operating mode ("normal mode") to the reduced heat generating mode ("low power mode") comprises disabling one or more subsystems (see column 7 lines 19-24, "disabling CPU cache memories, powering down portions") within the electronic device ("CPUs 12 and 14").

As per claim 15, the Osecky et al. reference discloses the one or more systems ("disabling CPU cache memories, powering down portions") comprise a cache memory (see column 7 lines 19-24, "cache memories").

As per claim 16, the Osecky et al. reference discloses the electronic device ("CPUs 12 and 14") comprises a data processor ("CPUs 12 and 14").

As per claim 17, the Osecky et al. reference discloses comprising monitoring a temperature (see column 7 lines 41-44, "monitor the temperature") of the electronic device ("CPUs 12 and 14") while the electronic device ("CPUs 12 and 14") continues to operate in the reduced heat generating mode ("low power mode").

As per claim 18, the Osecky et al. reference discloses displaying the temperature ("monitor the temperature") of the electronic device ("CPUs 12 and 14") on a display (see column 4 lines 43-51, "temperature bands") while operating the electronic device ("CPUs 12 and 14") in the reduced heat generating mode ("low power mode").

As per claim 19, the Osecky et al. reference discloses the display ("temperature bands") is located in a position where it is visible (see column 4 lines 43-51, "green, yellow, red") to a person (see column 7 lines 51-53, "operator") who is viewing the cooling system ("cooling devices 28 and 30") for the electronic device ("CPUs 12 and 14") through an access opening in a housing (see column 3 lines 40-41, "computer system 10").

As per claim 21, the Osecky et al. reference discloses causing the electronic device ("CPUs 12 and 14") to be shut down (see column 4 lines 49-51, "powered down") in the event that the temperature ("temperature") of the electronic device ("CPUs 12 and 14") reaches a threshold value (see column 4 lines 52-55, "critical temperature").

As per claim 22, the Osecky et al. reference discloses switching the electronic device ("CPUs 12 and 14") from the normal operating mode ("normal mode") to the reduced heat generating mode ("low power mode") upon a person (see columns 7-8 lines 65-2, "technician") initiating a first signal ("engaging in a replacement dialog") indicating that the person ("technician") is ready to service ("replacement") the cooling system (see column 7 lines 63-65, "failed cooling device").

As per claim 23, the Osecky et al. reference discloses switching the electronic device ("CPUs 12 and 14") from the reduced heat generating mode ("low power mode") to the normal operating mode ("normal mode") upon a person ("technician") initiating a second signal ("engaging in a replacement dialog") indicating that the person ("technician") has completed servicing (see column 8 lines 1-2, "replaced") the cooling system ("field replacement unit").

As per claim 24, the Osecky et al. reference discloses the first signal ("engaging in a replacement dialog") is generated in response to the person ("technician") activating a control ("engaging in a replacement dialog").

As per claim 25, the Osecky et al. reference discloses the first signal (see columns 7-8 lines 65-2, "contact switch") is generated in response to the person ("technician") disconnecting the cooling system ("failed cooling device") from a source of electrical power ("cooling device monitoring and control unit 32").

As per claim 26, the Osecky et al. reference discloses the first signal (see columns 7-8 lines 65-2, "contact switch") is generated in response to disconnection of the cooling system ("failed cooling device") from a source of electrical power ("cooling device monitoring and control unit 32") and the second signal ("contact switch") is generated in response to reconnection of the cooling system ("field replaceable unit") to the source of electrical power ("cooling device monitoring and control unit 32").

As per claim 27, the Osecky et al. reference discloses the cooling system ("failed cooling device") comprises a fan (see column 4 lines 6-9, "turbo cooler fan") and servicing the cooling system ("failed cooling device") comprises replacing the fan ("turbo cooler fan").

As per claim 28, the Osecky et al. reference discloses indicating the temperature (see column 7 lines 41-44, "temperature") of the electronic device ("CPU") by way of an audible signal (see column 7 lines 51-53, "audio signal") while operating the electronic device ("CPU") in the reduced heat generating mode ("low power mode").

As per claim 29, the Osecky et al. reference discloses the cooling system ("failed cooling device") comprises a fan (see column 4 lines 6-9, "turbo cooler fan") and servicing the cooling system ("failed cooling device") comprises replacing the fan ("turbo cooler fan").

As per claim 30, the Osecky et al. reference discloses a method for servicing apparatus which includes a cooling system for an electronic device, the method comprising: operating the apparatus (see column 3 lines 40-41, "computer system 10") in a temperature control mode (see column 3 lines 55-58, "low power mode") in which temperature rise in the electronic device ("CPU") is reduced; continuing to operate the apparatus ("computer system 10") in the temperature control mode ("low power mode") while the cooling system (see column 4 lines 6-10, "cooling devices 28, 30 ") is being serviced (see column 7 lines 47-62, "operator

notification"); and subsequently switching the apparatus ("computer system 10") back to a normal operating mode (see column 8 lines 26-28, "normal mode").

As per claim 31, the Osecky et al. reference discloses electronic apparatus comprising: a heat generating electronic device (see column 3 lines 41-42, "CPUs 12 and 14"); a cooling system (see column 4 lines 6-10, "cooling devices 28, 30") operational to cool the electronic device ("CPUs 12 and 14"); a maintenance procedure controller (see column 4 lines 17-19, "cooling device monitoring and control unit 32") configured to: switch the electronic device ("CPUs 12 and 14") from a normal operating mode (see column 8 lines 26-28, "normal mode"), wherein the electronic device ("CPUs 12 and 14") generates heat, to a reduced heat generating mode (see column 3 lines 55-58, "low power mode"), wherein the electronic device ("CPUs 12 and 14") generates heat at a reduced rate, upon detection of a signal (see column 5 lines 25-30, "signals") indicating that the cooling system ("cooling device failure") is about to be serviced (see column 7 lines 47-62, "operator notification"); and switch the electronic device ("CPUs 12 and 14") from the reduced heat generating mode ("low power mode") to the normal operating mode ("normal mode") upon detection of a signal (see columns 7-8 lines 65-2,

"replacement dialog, contact switch") indicating that servicing ("replacement") of the cooling system ("field replaceable unit") has been completed ("replaced").

As per claim 32, the Osecky et al. reference discloses a clock generator ("CPUs") operative to generate a clock signal (see column 7 lines 20-21, "clock speed") supplied to the electronic device ("CPUs").

As per claim 33, the Osecky et al. reference discloses the maintenance procedure controller (see columns 63-2, "cooling device monitoring and control unit 32") is connected to control a frequency of the clock signal (see column 7 lines 20-21, "reducing the clock speed").

6. Claims 1, 2, 5-8, 10, 12, 17, 20 and 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by USPN 6,704,875 B2 to Kinoshita et al.

As per claim 1, the Kinoshita et al. reference discloses a method for servicing a cooling system for an electronic device, the method comprising: switching the electronic device (see column 2 lines 52-55, "processor 11") from a normal operating mode (see column 4 lines 37-43, "normal mode") wherein the electronic device ("processor 11") generates heat to a reduced heat generating mode (see column 2 lines 52-55, "low-electric-power consumption mode") wherein

the electronic device ("processor 11") generates heat at a reduced rate; continuing to operate the electronic device ("processor 11") in the reduced heat generating mode ("low-electric-power consumption mode") while the cooling system (see column 3 lines 26-32, "fan") is being serviced ("fan stop signal"); and subsequently switching the electronic device ("processor 11") from the reduced heat generating mode ("low-electric-power consumption mode") to the normal operating mode ("normal mode").

As per claim 2, the Kinoshita et al. reference discloses switching the electronic device ("processor 11") from the normal operating mode ("normal mode") to the reduced heat generating mode ("low-electric-power consumption mode") comprises reducing a clock frequency (see column 4 lines 33-37, "clock processing") applied to the electronic device ("processor 11").

As per claim 5, the Kinoshita et al. reference discloses switching the electronic device ("processor 11") from the normal operating mode ("normal mode") to the reduced heat generating mode ("low-electric-power consumption mode") comprises operating the electronic device ("processor 11") at a reduced duty cycle (see column 6 lines 58-61, "75%, 50%").

As per claim 6, the Kinoshita et al. reference discloses switching the electronic device ("processor 11") from the normal operating mode ("normal mode") to the reduced heat generating mode ("low-electric-power consumption mode") comprises operating the electronic device ("processor 11") at a reduced duty cycle (see column 6 lines 58-61, "75%, 50%").

As per claim 7, the Kinoshita et al. reference discloses operating the electronic device ("processor 11") at a reduced duty cycle ("75%, 50%") comprises operating the electronic device ("processor 11") at a duty cycle of 25% or less (see column 5 lines 31-33, 39-41, "rate of dropping an operating speed").

As per claim 8, the Kinoshita et al. reference discloses operating the electronic device ("processor 11") at a reduced duty cycle ("75%, 50%") comprises issuing an alternating sequence of HALT (see column 4 lines 33-37, 50-55, "performs minimum processing required for resuming control operation") and RESTART (see column 4 lines 37-39, 50-55, "perform processing related to axes control") commands to the electronic device ("processor 11").

As per claim 10, the Kinoshita et al. reference discloses operating the electronic device ("processor 11") at a reduced duty cycle ("75%, 50%") also

comprises reducing the duty cycle ("75%, 50%") by way of a mechanism (see column 4 line 49, "switching of modes") built into the electronic device ("processor 11").

As per claim 12, the Kinoshita et al. reference discloses operating the electronic device ("processor 11") at a reduced duty cycle ("75%, 50%") comprises reducing the duty cycle ("75%, 50%") by way of a mechanism (see column 4 line 49, "switching of modes") built into the electronic device ("processor 11").

As per claim 17, the Kinoshita et al. reference discloses comprising monitoring a temperature (see column 3 lines 23-26, "temperature sensor TS") of the electronic device ("processor 11") while the electronic device ("processor 11") continues to operate in the reduced heat generating mode ("low-electric-power consumption mode").

As per claim 20, the Kinoshita et al. reference discloses at least in part on the basis of the monitored temperature ("temperature sensor TS"), computing an estimated time (see column 6 lines 54-57, "time") until the temperature ("detected temperature Tr") of the electronic device ("processor 11") reaches a threshold value (see column 5 lines 26-38, "thresholds TI, T2, T3") and displaying the estimated time (see columns 6-7 lines 67-15, "times t1, t2").

As per claim 31, the Kinoshita et al. reference discloses electronic apparatus comprising: a heat generating electronic device (see column 2 lines 52-55, "processor 11"); a cooling system (see column 3 lines 26-32, "fan") operational to cool the electronic device ("processor 11"); a maintenance procedure controller ("processor 11") configured to: switch the electronic device ("processor 11") from a normal operating mode (see column 4 lines 37-43, "normal mode"), wherein the electronic device ("processor 11") generates heat, to a reduced heat generating mode (see column 2 lines 52-55, "low-electric-power consumption mode"), wherein the electronic device ("processor 11") generates heat at a reduced rate, upon detection of a signal (see column 3 lines 30-32, "fan stop signal") indicating that the cooling system ("fan") is about to be serviced ("fan stop signal"); and switch the electronic device ("processor 11") from the reduced heat generating mode ("low-electric-power consumption mode") to the normal operating mode ("normal mode") upon detection of a signal (see column 3 lines 26-32, "fan stop signal") indicating that servicing of the cooling system ("fan") has been completed.

As per claim 32, the Kinoshita et al. reference discloses a clock generator ("processor 11") operative to generate a clock signal (see column 4 lines 33-37, "clock processing") supplied to the electronic device ("processor 11").

As per claim 33, the Kinoshita et al. reference discloses the maintenance procedure controller ("processor 11") is connected to control a frequency of the clock signal ("clock processing").

As per claim 34, the Kinoshita et al. reference discloses the maintenance procedure controller ("processor 11") is connected to control a duty cycle (see column 6 lines 58-61, "75%, 50%") of the electronic device ("processor 11").

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,792,550 B2 to Osecky et al. in view of US Pub. No. 2002/0188875 A1 to Hwang et al.

As per claim 3, the Osecky et al. reference does not expressly disclose reducing the clock frequency applied to the electronic device comprises reducing the clock frequency by 85% or more.

The Hwang et al. reference discloses

(see page 5 [0082], "In a typical 1000 Mbit mode, the PHY clock operates at 125 MHz, the GMAC clock operates at 62.5 MHz, the core clock operates at 66 MHz and the CPU clock operates at 133 MHz. When the device is forced to operate in the 10 Mbit mode, the PHY clock may operate at 2.5 MHz, the GMAC clock may operate at 2.5 MHz, the core clock may operate at 12.5 MHz, and the CPU clock may operate at 25 MHz. These reduced clock speeds cause the integrated circuit to substantially reduce its power consumption.")

(see page 6 [0086], "... the clock controller 130 generates the 25 MHz CPU clock 212 and the 12.5 MHz core clock 214 from the 25 MHz clock 102.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the low power mode as taught by the Osecky et al. reference to include reducing the clock speed substantially as taught by the Hwang et al.

One of ordinary skill in the art would have been motivated to modify the low power mode to include reducing the clock speed substantially so that the reduced clock speeds caused the CPU to substantially reduce its power consumption depending on the power budget of the system.

9. Claims 9 and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,704,875 B2 to Kinoshita et al. in view of USPN 6,088,807 to Maher et al.

As per claim 9, the Kinoshita et al. reference does not expressly disclose issuing the alternating sequence of HALT and RESTART commands to the electronic device comprises toggling a logic signal applied to a halt pin on the electronic device.

The Maher et al. reference discloses

(see column 6 lines 25-32, "... the operation of the microprocessor 12 may be suspended responsive to a software command ... a "HALT" operation ... stops execution of all instructions ... Execution is resumed responsive to a non-maskable interrupt (on the NMI pin) coupled to the bus controller 40, an unmasked interrupt (on the INT pin coupled to the bus controller 40) or a RESET.")

(see column 6 lines 35-40, "... the HALT instruction has essentially the same consequence as asserting the SUSP pin ... the BIOS 16 can issue a HALT instruction to the microprocessor 12, thereby disabling CLKB ... a significant reduction of power consumed by the microprocessor 12.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the switching of modes as taught by the Kinoshita et al. reference with the HALT operation as taught by the Maher et al. reference to illustrate a method of reducing power consumption.

One of ordinary skill in the art would have been motivated to modify the switching of modes with the HALT operation to illustrate a method of reducing power consumption to prevent thermal runaway and thermal destruction of the processor.

As per claim 35, the rejection of claim 9 is incorporated and further claim 35 contains limitations recited in claim 9; therefore claim 35 is rejected under the same rationale as claim 1.

10. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,704,875 B2 to Kinoshita et al. in view of USPN 6,088,807 to Maher

et al. as applied to claims 9 and 35 above, and further in view of US Pub. No. 2003/0204758 A1 to Singh.

As per claims 11 and 13, the Kinoshita et al. reference does not expressly disclose the mechanism built into the electronic device comprises a mechanism operating according to the Advanced Configuration and Power Interface standard.

The Singh reference discloses

(see page 3 [0036], "The total power consumed by CPU 204 depends on a number of parameters such as the clock frequency at which a processor is running, the duty cycle, the number of processors active in the system, etc. ... manager 280 reduces and/or adjusts one or a plurality of the above parameters to reduce the power consumed by CPU 204 ... Manager 280, when appropriate, also sets this duty cycle to zero, which effectively halts CPU 204 even though it is still powered on ... manager 280, through an application using the ACPI interface, turns off CPU 204 implemented by the Intel's processor chips and board designs ... manager 280 via a CPU board interface reduces the clock speed driving CPU 204.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of switching modes as taught by the Kinoshita et al. reference to include the ACPI interface as taught by the Singh

reference to power down a processor depending on its processor chips and board designs.

One of ordinary skill in the art would have been motivated to modify the method of switching modes to include the ACPI interface to power down a processor depending on its processor chips and board designs to facilitate interfacing with various processor chips and board designs.

Allowable Subject Matter

11. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to power conservation in general:

USPN 6,873,883 B2 to Ziarnik

USPN 6,859,882 B1 to Fung

USPN 6,528,974 B1 to Mirov et al.

USPN 6,526,333 B1 to Henderson et al.

USPN 6,446,215 B1 to Meyer et al.

USPN 5,842,029 to Conary et al.

US Pub. No. 2004/0236975 A1 to Gaskins et al.

US Pub. No. 2004/0204016 A1 to Sakamoto

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 571.272.3679. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 571.272.3687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Crystal J Barnes

CJB
17 June 2005